UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/815,083	03/31/2004	Salman Akram	97-1363.5	7356

22823 7590 05/23/2005

STEPHEN A GRATTON
THE LAW OFFICE OF STEVE GRATTON
2764 SOUTH BRAUN WAY
LAKEWOOD, CO 80228

EXAMINER	
THAI, LUAN C	

ART UNIT	PAPER NUMBER
2891	

DATE MAILED: 05/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/815,083	AKRAM ET AL.	
	Examiner	Art Unit	
	Luan Thai	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *78-108* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *78-108* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/31/04&9/7/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. This application appears to be a continuation of Application No. 09/961,646, filed 9/25/01.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the recitations "forming insulating layers in the opening" in claim 105 and "the conductive members comprise layers of solder on sidewalls of the opening" in claim 103 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 78-81, 90-95, 99-102 and 106-107 are rejected under 35 U.S.C. 102(e) as being anticipated by Sarkhel et al. (5,874,043) and Brusic et al. (5,960,251), separately.

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 78-81, 90-95, 99-102 and 106-107, Sarkhel et al. (see specifically figure 3) disclose a method for fabricating a semiconductor component comprising: providing a substrate (34) having a first side and a second side; forming a plurality of openings (36) in the substrate extending from the first side to the second side; and forming conductive members in the openings by exposing the openings to solder plugs (31) which completely fill the openings (36), wherein the forming the conductive members step is performed using a solder wave (Col. 5, lines 17+) in order to provide capillary action (Col. 5, lines 23+). Sarkhel et al. further disclose forming a plurality of first contacts (40) on the first side in electrical communication with the conductive members (31) and forming a plurality of second contacts (41) on the second side in electrical communication with the conductive members (31).

Brusic et al. (see figure 7-8, Col. 7, lines 55-67, Col. 8, lines 1-9) also teaches a method for fabricating a semiconductor component identical to Sarkhel et al.'s method; therefore, claims 78-81, 90-95, 99-102 and 106-107 are also rejected under 35 U.S.C. 102(e) as being anticipated by Brusic et al. for the similar reasons detailed above.

5. Claims 78, 81-84, 86-87, 90, 93, 97-99, 102 and 108 are rejected under 35 U.S.C. 102(b) as being anticipated by Tanielian (5,166,097).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 78, 81-84, 86-87, 90, 93, 97-99, 102 and 108, Tanielian (see specifically figures 1-6) discloses a method for fabricating a semiconductor component

comprising: providing a silicon wafer substrate (2) having a first side and a second side; forming a plurality of openings (10) in the substrate extending from the first side to the second side by dry etching process (Col. 4, lines 32+); forming conductive members in the openings. Tanielian further discloses forming a plurality of first and second contacts (32) on the first and second sides in electrical communication with the conductive members (16).

6. Claims 78, 81, 85-90, 93-95, 99, 102, 104, and 106-107 are rejected under 35 U.S.C. 102(b) as being anticipated by Leary-Renick (4,622,058).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 78, 81, 85-90, 93-95, 99, 102, 104, and 106-107, Leary-Renick (see specifically figures 2 and 4A) discloses a method for fabricating a semiconductor component comprising: providing a substrate (80) having a first side and a second side; forming a plurality of openings in the substrate by laser machining and dry etching (Col. 2, lines 46+), wherein the openings are extended from the first side to the second side and filled by conductive members (82). Leary-Renick further disclose forming a plurality of first and second contacts (88) on the first and second sides in electrical communication with the conductive members (82).

7. Claims 78, 81, 90, 93-96, 99, and 102-107 are rejected under 35 U.S.C. 102(e) as being anticipated by Koh et al. (5,599,744).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 78, 81, 90, 93-96, 99, and 102-107, Koh et al. (see specifically figures 1-3-5) discloses a method for fabricating a semiconductor component comprising: providing a

substrate (10) having a first side and a second side; forming a plurality of openings (12) in the substrate by laser machining (Col. 7, lines 32+), wherein the openings are extended from the first side to the second side and filled by conductive solder plug (20). Koh et al. further disclose solder layers (14-15-16) on the sidewalls of the openings (12) (see figures 1-3). Koh et al. also disclose insulating layers (18) being formed prior to the forming of the conductive plug (20). Koh et al. further teach a plurality of first and second contacts (e.g., the expanded flat portions at two ends of the conductive plug 20) on the first and second sides of the substrate (10) and in electrical communication with the conductive plug (20).

8. Claims 78-79, 81, 90, 92-95, 99, 101-102 and 106-107are rejected under 35 U.S.C. 102(b) as being anticipated by Bitaillou et al. (4,830,264).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 78-79, 81, 90, 92-95, 99, 101-102 and 106-107, Bitaillou et al. (see specifically figures 2-3) disclose a method for fabricating a semiconductor component comprising: providing a substrate (11) having a first side and a second side; forming a plurality of openings (14) in the substrate extending from the first side to the second side; and forming conductive members in the openings by exposing the openings to solder plugs (19) which completely fill the openings (14) by capillaries (Col. 6, lines 45+). Bitaillou et al. further disclose a plurality of first and second contacts (22) (23) respectively formed on the first and second sides of the substrate, in electrical communication with the conductive members (19).

9. Claims 78, 81, 85-90, 93-95, 99, 102-104 and 106-107 are rejected under 35 U.S.C. 102(b) as being anticipated by Lynch (4,954,313).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 78, 81, 85-90, 93-95, 99, 102-104 and 106-107, Lynch (see specifically figures 1-4) disclose a method for fabricating a semiconductor component comprising: providing a substrate (20) having a first side and a second side; forming a plurality of openings (22) in the substrate extending from the first side to the second side; and forming conductive members in the openings by exposing the openings to metal solder or solder plugs (42) which completely fill the openings (22) by etching and laser machining (Col. 3, lines 44+). Lynch further disclose the conductive members comprising solder layers (30-32-34) on sidewalls of the openings (see figure 3C), and a plurality of first and second contacts (42) respectively formed on the first and second sides of the substrate, in electrical communication with the conductive members (see figure 4C).

10. Claims 78-81, 90-95, 99-102 and 106-107 are rejected under 35 U.S.C. 102(e) as being anticipated by Brusic et al. (5,960,251).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 78-81, 90-95, 99-102 and 106-107, Brusic et al. (see specifically figure 3) disclose a method for fabricating a semiconductor component comprising: providing a substrate (34) having a first side and a second side; forming a plurality of openings (36) in the substrate extending from the first side to the second side; and forming conductive members in the openings by exposing the openings to solder plugs (31) which completely fill the openings (36), wherein the forming the conductive members step is performed using a solder wave (Col. 5,

lines 17+) in order to provide capillary action (Col. 5, lines 23+). Brusic et al. further disclose forming a plurality of first contacts (40) on the first side in electrical communication with the conductive members (31) and forming a plurality of second contacts (41) on the second side in electrical communication with the conductive members (31).

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luan Thai whose telephone number is 571-272-1935. The examiner can normally be reached on 6:30 AM - 5:00 PM, Monday to Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bradley W. Baumeister can be reached on 571-272-1722. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Thai/

Luan Thai
Primary Examiner
Art Unit 2891
May 19, 2005